Introduction:

A boost converter is a DC-DC converter that steps up an input voltage with a very high efficiency. This converter is widely used in many applications, including active power factor correction circuits, EV battery chargers, LED drivers, and more. It is becoming increasingly necessary to find methods to convert AC or DC voltage of all levels to other AC or DC voltages of a different level efficiently and cheaply. The boost converter built in this course will serve to demonstrate the practical application of the knowledge and skills obtained in this course. A boost converter will be designed using first principles and mathematical models, simulated and optimized in SPICE, then built, tested, and compared with the theoretical model.

Theory of Operation:

Unlike its electrical dual, the buck converter, which steps down an input voltage by chopping it at precise intervals and filtering the output using a second-order LC filter, a boost converter is more accurately described as a *current chopper* and can be theoretically modeled with the schematic shown in Figure 2.1.

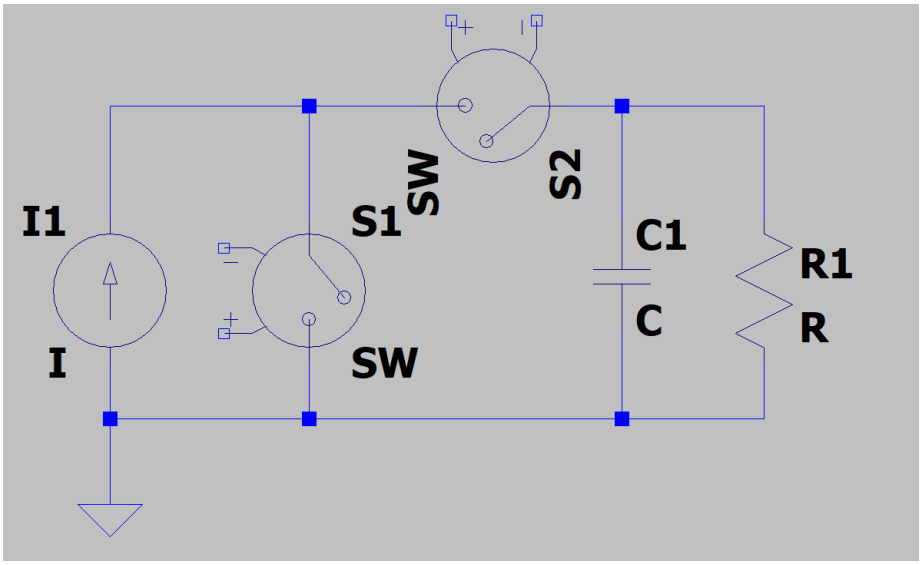

Figure 2.1: A theoretical model of a boost converter

By precisely controlling the amount of time DT, where D is the duty cycle as a percentage of time and T is the period of the pulses in seconds, in which the current is allowed to flow from the input to the output, the output current is decreased and as a consequence, the output voltage is increased. However, in practice a current source is difficult to obtain, so the schematic of the boost converter is modified to contain an inductor in series with a voltage source and the ideal switches have been realized with their semiconductor counterparts as shown in Figure 2.2. Note how diode D1 could easily be replaced with another MOSFET, making it a *synchronous* boost converter and gaining a little bit more efficiency.

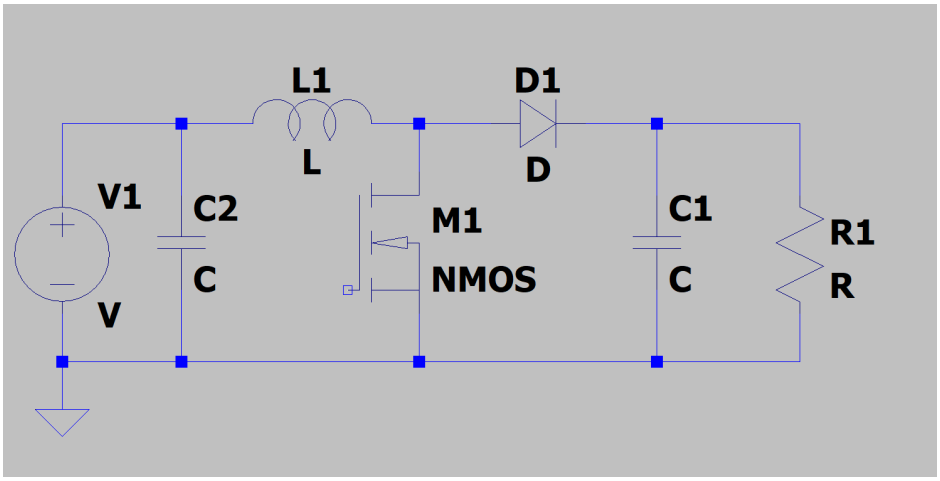

Figure 2.2: A practical boost converter

The boost converter's voltage conversion ratio can be calculated using the method of inductor charge-balancing. The average voltage across an inductor must be zero during steady state operation, otherwise the current through the inductor will keep on increasing until destruction. Given that there are two switches, a total of 4 switch configurations are possible (Table 2.3).

MOSFET	Diode
OFF	OFF
ON	OFF
OFF	ON
ON	ON

Table 2.3: Possible switch states of the boost converter.

Assuming the converter is in periodic steady-state, each case was considered to deduce their possibility:

Case 1: If both the MOSFET and diode are off, the current that was already flowing in the inductor will suddenly drop to zero, as the current will have nowhere to go. The voltage across the inductor is given by the formula $V = L\frac{di}{dt}$, and if the change of current is big, the inductor will create a large positive voltage, forward-biasing the diode, forcing it to turn on. This means that this state is impossible.

Case 2: If the MOSFET is on and the diode is off, the diode will be reverse-biased meaning that it will be off and the MOSFET will simply direct current from the voltage source, through the inductor, and to ground. This state is perfectly acceptable.

Case 3: Case 1 automatically goes to this state, indicating that this is indeed a stable, possible state.

Case 4: If both the MOSFET and diode are on, the diode will again be reverse biased, forcing the diode to turn off and returning to Case 2. This case is impossible.

Now that it has been proven that there are only two stable states of this circuit, the inductor charge-balance equation can be written. Assuming that the MOSFET is on for time DT and off for time (1-D)T, the voltage across the inductor can be modeled as:

$$V_L = V_{in}D + (V_{in} - V_{out})(1 - D)$$

Setting this equation to 0 for steady-state operation and solving for $\frac{V_{out}}{V_{in}}$ gives the theoretical conversion ratio of an ideal boost converter: $\frac{V_{out}}{V_{in}} = \frac{1}{1-D}$.

However, the perfect boost converter does not exist, and it is necessary to take into account the equivalent series resistance (ESR) of the inductor, typical forward voltage drop of the diode (V_F), and the drain-to-source on resistance of the MOSFET (R_{DS_ON}), which can be modeled by adding two resistors in series with the inductor and the MOSFET as well as a voltage source to represent the diode voltage drop (Figure 2.4). Resistor R4 represents the load.

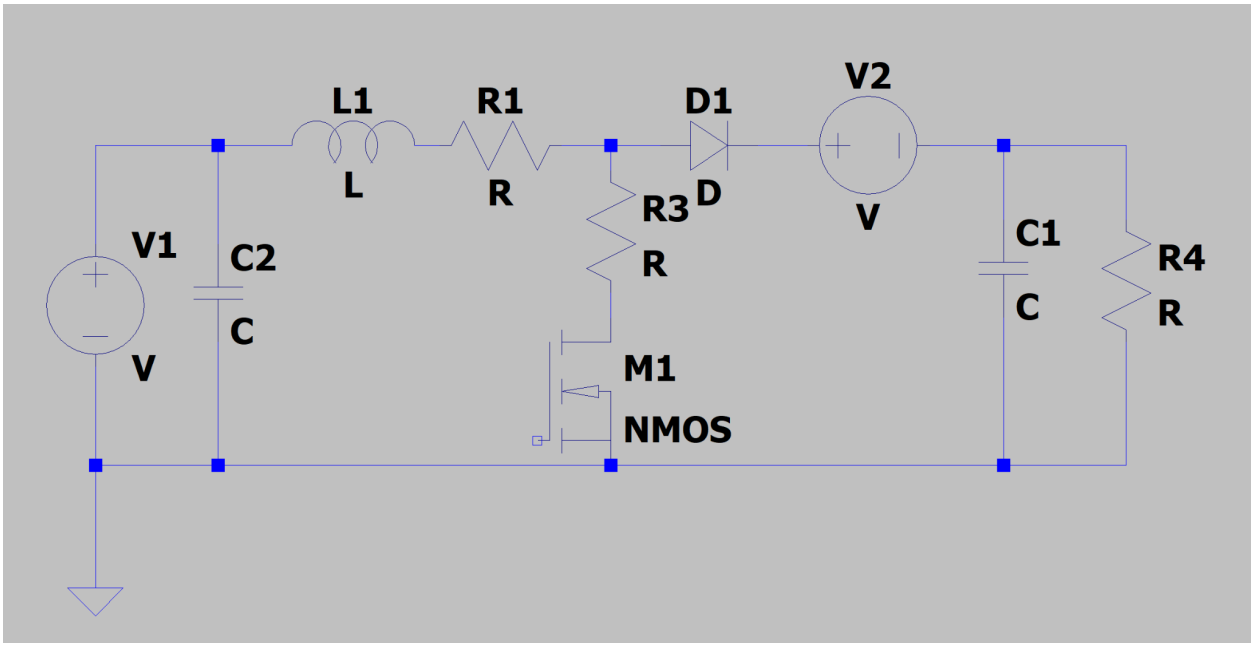

Figure 2.4: Better approximation of a real boost converter.

The voltage conversion ratio will have to be recalculated again using inductor and capacitor charge-balance. The equations describing the voltage and currents of the converter over one complete period are as follows:

(1) $$V_L = (V_{in} - I_L(R_{ESR} + R_{DS-ON}))D + (V_{in} - I_L R_{ESR} - V_F - V_{out})(1 - D)$$

(2) $$I_{C_2} = I_{in} - I_L$$

(3) $$I_{C_1} = -\frac{V_{out}}{R_{Load}}D + (I_L - \frac{V_{out}}{R_{Load}})(1 - D)$$

Using these equations, it is possible to calculate the inductor size or switching frequency needed to obtain a certain output voltage ripple and inductor current ripple. Applying capacitor charge balance to equations 2 and 3 gives us the following results:

$$I_L = I_{in}$$

$$I_L = I_{out}(\frac{1}{1-D}) = \frac{V_{out}}{R_{Load}}(\frac{1}{1-D}) \rightarrow I_{in} = I_{out}(\frac{1}{1-D})$$

Substituting these values into equation 1 and charge-balancing the inductor gives:

(4) $$V_{out} = \frac{V_{in} - V_F(1-D)}{(\frac{R_{ESR}}{R_{Load}(1-D)} + \frac{R_{DS-ON}D}{R_{Load}(1-D)} + (1-D))}$$

It can be seen that if V_F was set to 0V and the parasitic resistances were all eliminated, this equation takes on the form of the conversion formula for the ideal boost converter. Figure 2.5 shows the graph of the output voltage vs duty cycle of the practical boost converter with a 12V input and an 8 ohm load compared with the ideal boost converter conversion function.

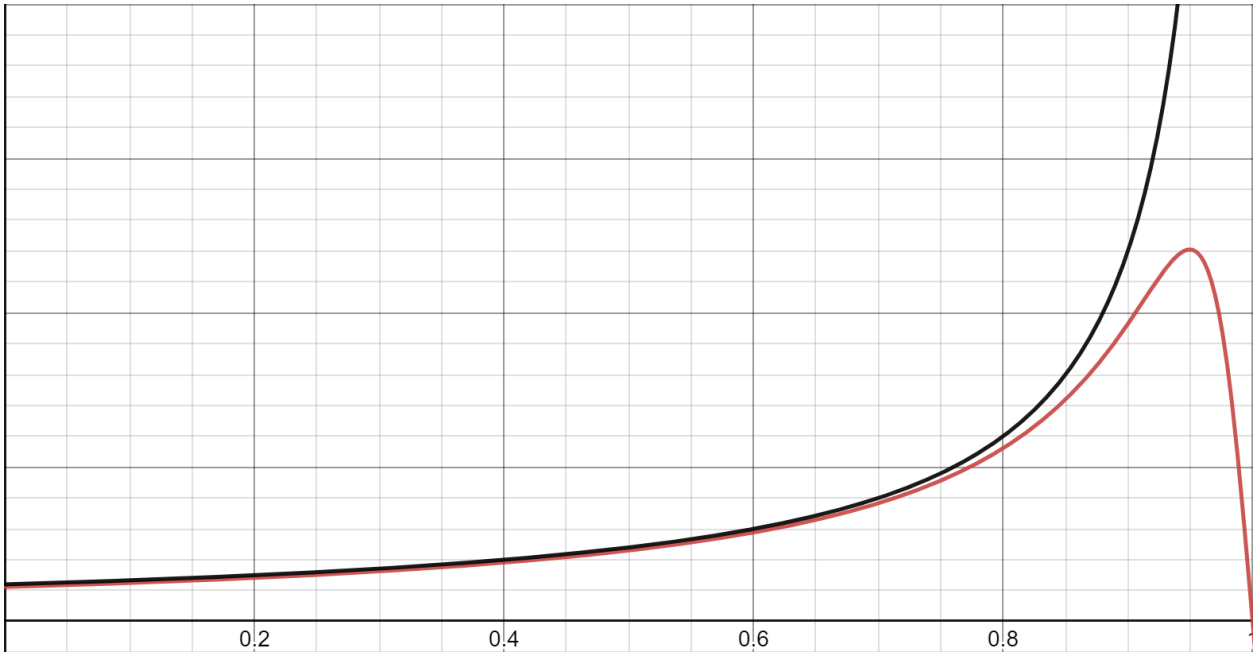

Figure 2.5: Ideal boost converter (purple) vs real boost converter (red)

Other factors of interest include the inductor current ripple and the output voltage ripple. The inductor current ripple can be calculated by analyzing the voltage across it:

$$V_L = L\frac{di}{dt}$$

$$\frac{di}{dt} = \frac{(V_{in} - \frac{V_{out}}{R_{Load}}(R_{ESR}+R_{DS-ON}))}{L}$$

(5) $\Delta i_{L,\,ripple} = \frac{1}{2}\frac{di}{dt}DT = \frac{(V_{in} - \frac{V_{out}}{R_{Load}}(R_{ESR}+R_{DS-ON}))}{2L}(\frac{D}{f})$, where f is the switching frequency

The output voltage ripple is dependent on the charge that is stored in the capacitor. Ideally, all of the current ripple in the inductor will get absorbed by the capacitor, so the voltage ripple will simply be a function of the amount of charge contained in the current ripple:

$$i = C\frac{dV}{dt} \rightarrow \Delta v_{c,\,ripple} = \frac{1}{C}\int i(t)\,dt$$

The shape of the inductor current is a triangle wave that oscillates around a non-zero positive average current, so the integral of the current simply equates to taking the area underneath the triangle above the average current.

(6) $$\Delta v_{c,\,ripple} = \frac{1}{C}\left(\frac{T}{2}\Delta i_{L,\,ripple}\right) = \frac{D\left(V_{in} - \frac{V_{out}}{R_{Load}}\left(R_{ESR} + R_{DS-ON}\right)\right)}{4f^2LC}$$

Design Specifications and Considerations for the Construction of a Practical Boost Converter:

The boost converter designed for this project has two requirements:

1. It must boost 12V to 24V±1% as efficiently as possible
2. The output voltage ripple must be less than 1% of output voltage

For this assignment, 6 different types of inductors were given to us along with a pre-chosen MOSFET, diode, and a prefabricated PCB. The ESRs of the inductors along with their inductances at three different frequencies were recorded (Table 3.1).

Inductor #	Measured Inductance (μH)			Measured ESR (mΩ)
	200 kHz	500 kHz	2 MHz	
1	2.05	2.02	2.08	156
2	0.150	0.150	0.147	0.800
3	0.800	0.800	0.795	5.17
4	1.38	1.35	1.34	16.9
5	17.8	17.3	17.7	20.2
6	4.59	4.59	4.59	4.49

Table 3.1: Inductor values

From an efficiency standpoint, it makes the most sense to choose the inductor with the lowest ESR which should lead to the lowest amount of I^2R losses, but it is also important to take switching losses into account as well. Generally, switching losses are going to be higher when

the MOSFET is switched at a higher frequency and when the MOSFET is being hard-switched. Hard switching is when a switch is turned off while there is still current passing through it, and since this boost converter is going to run in continuous conduction mode (CCM)-- meaning the current in the inductor will not fall to zero during steady-state operation– the MOSFET will be hard-switched the entire time. Thus, lower switching frequencies are desirable.

Table 3.1 reveals that inductor #2 has the lowest ESR, but also a very small inductance, which means the switching frequency will need to be increased in order to maintain a small output voltage ripple, according to equation 6. So an inductor must be chosen with both its ESR and inductance in consideration. A non-standard metric defined by the ratio between an inductor's inductance and its ESR has been created for this project that provides a quantitative value for finding the inductor that minimizes efficiency and maximizes inductance (Table 3.2).

Inductor #	**Inductance/ESR (H/Ω)**
1	1.31×10^{-5}
2	1.86×10^{-4}
3	1.55×10^{-4}
4	8.02×10^{-5}
5	8.72×10^{-4}
6	1.02×10^{-3}

Table 3.2: Inductance per ohm for each inductor

From Table 3.2, it is clear that inductor #6 is by far the best choice, as it provides the best balance between inductance and ESR. That inductor is the Coilworks MLC1565-472ML inductor, a commercially available power inductor featuring the following relevant properties obtained from its datasheet:

Saturation Current for 10% drop in inductance	6.23A
Saturation Current for 20% drop in inductance	10.57A

This design aims to limit the inductance drop to around 10%, limiting the maximum input current to around 6A, and by the conservation of energy:

$$V_{in}I_{in} = V_{out}I_{out} \rightarrow 12V * 6A = 24V * 3A \rightarrow I_{out} = 3A$$

The load resistor value can be calculated using Ohm's law:

$$V = IR \rightarrow 24 = 3R \rightarrow R = 8\Omega$$

The MOSFET used in the boost converter is a gallium nitride (GaN) N-channel enhancement MOSFET called the GaN GS61004 with the following important properties:

Maximum V_{GS}	6V
Maximum V_{DS}	100V
Maximum I_{DS}	38A
$R_{DS\text{-}ON}$	16 mΩ
Gate charge	3.3nC

The diode in the boost converter will be made up of a pair of PMEG100T200ELPE Schottky diodes in parallel, each with the following relevant properties:

Average Max Forward Current (I_F)	20A
Reverse Voltage (V_R)	100V
Max Forward Voltage Drop (V_F)	840mV

Capacitor values were limited to what was in stock and the amount of PCB space given. Since there were only 8 pads for the input capacitors and 7 pads for the output capacitors, and the only capacitors available with a high enough voltage rating were 4.7μF 100V capacitors, this

limited the input capacitance to a maximum of 37.6μF and the output capacitance to a maximum of 32.9μF.

These values derived from the datasheet not only provide the values necessary for calculating the voltage conversion ratio and the expected voltage and current ripples, but also the amount of performance to expect from the boost converter without overstressing the components. The preliminary performance values shown in Table 3.3 are calculated from the values derived from the datasheets and assumed values.

Input Voltage	12V
Switching Frequency	500 kHz
Input Capacitance	18.8μF
Inductor Value	4.59μH
Output Capacitance	32.9μF
Output Load Resistor	8 Ω
Duty Cycle	52%
Expected Output Voltage	23.99V
Expected Inductor Current Ripple	1.35A
Expected Output Voltage Ripple	41.11mV

Table 3.3: Final chosen values for the input and components of the boost converter and its expected performance based on the derived formulas.

According to the formulas, this boost converter will meet the specifications set out in the beginning of the section. However, it is important to note that these values do not take switching losses or other subtle details about the components, thus the actual performance may vary. Hence, SPICE simulation is needed to obtain even more accurate results.

SPICE simulation:

The SPICE model for the MOSFET and diode can be obtained from their respective manufacturers' websites. After the SPICE models were downloaded and incorporated into the design, many optimizations were made in an attempt to obtain even higher efficiencies by adjusting the load value, duty cycle, MOSFET gate drive resistance, etc. The SPICE model created in Figure 4.1 resembles the actual circuit design given to us on the PCB.

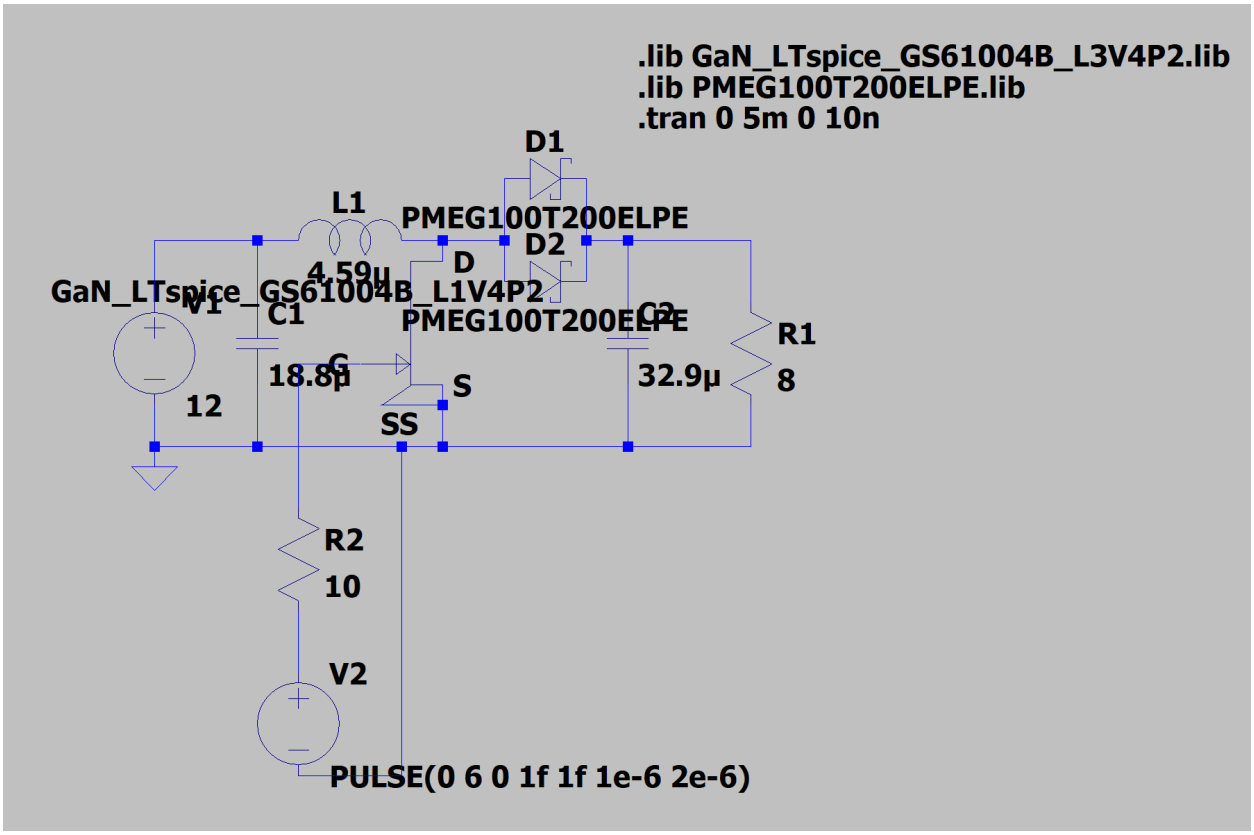

Figure 4.1: SPICE model of the boost converter. Note the paralleled diodes and the special MOSFET model.

The results of this initial simulation are shown in Figure 4.2 and the extrapolated values are given in Table 4.3. Note that the green trace is the output voltage and that the input current is negative of what it actually is.

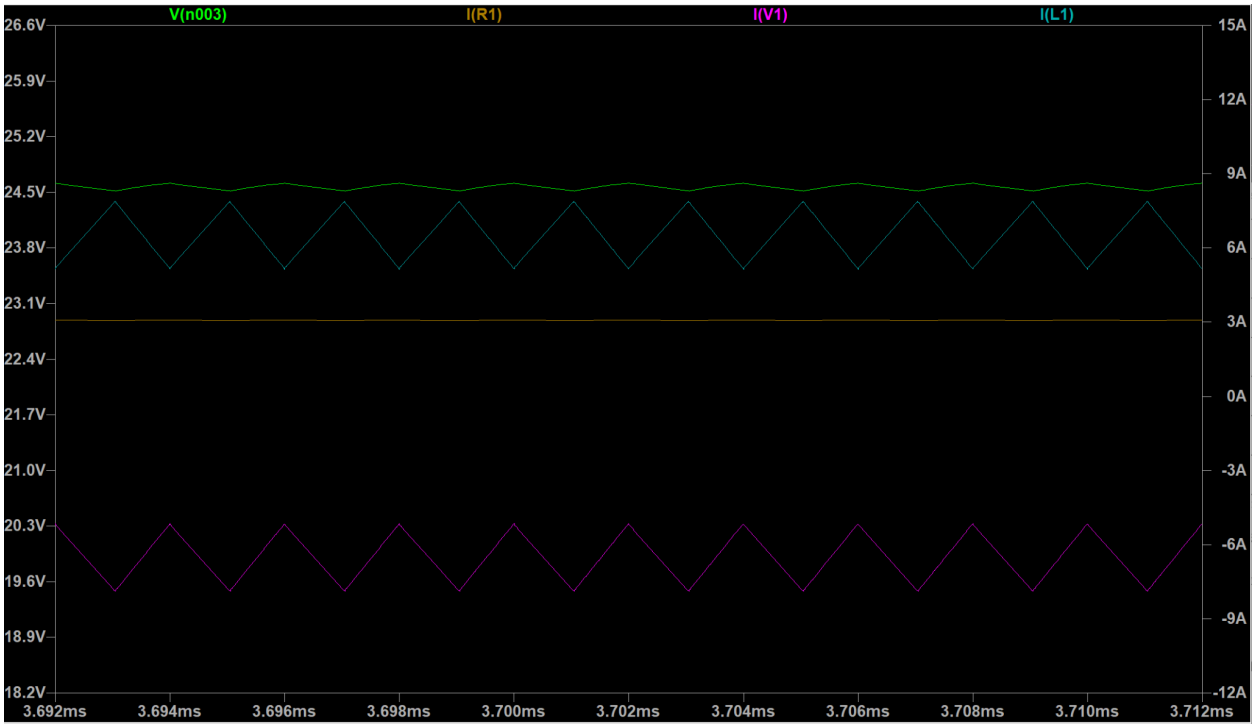

Figure 4.2: SPICE results of the initial boost converter design

Input Voltage	12V	
Input Current (RMS)	6.5695A	
Output Voltage (RMS)	24.568V	2.4% difference
Output Current (RMS)	3.071A	
Output Voltage Ripple	49.36mV	20.1% difference
Inductor Current Ripple	1.378A	2.1% difference
Efficiency	95.71%	

Table 4.3: Extrapolated values from the simulation and % deviation from calculated values

The values obtained from the simulation are very close but do not exactly match the calculated values because the simulation also takes into account the switching losses. Though the initial design made it seem like the boost converter was in spec, the simulation results show that the output voltage has fallen a little bit out of spec. This can be attributed to the fact that the maximum diode forward voltage drop was used when calculating the conversion ratio formula and in reality, this might not be the case. Thus, a simple solution will be to drop the duty cycle a

little bit to get the voltage back within spec. Since it has been verified that the boost converter design meets the specifications, methods of iterative design will be used to increase the efficiency of the circuit.

Increasing Efficiency:

In theory, the most obvious efficiency improvement is to decrease the gate resistor on the MOSFET. The resistor is there to increase the amount of time that it takes for the gate driver to charge the input capacitance of the gate in order to limit the amount of voltage spikes due to LC oscillations caused by the parasitic inductances and capacitances. However, this increased gate charging time will lead to a slower turn-on time for the MOSFET, increasing the amount of time the MOSFET spends in saturation mode, and decreasing the efficiency. Three efficiency tests were run on the SPICE model, each with decreasing gate resistance, in order to confirm if a smaller gate resistance will lead to a higher efficiency (Table 5.1).

5Ω	95.76%
3Ω	95.75%
1Ω	95.80%

Table 5.1: Efficiency of the boost converter with varying MOSFET gate resistances.

The results do confirm the theory that generally a smaller gate resistance will lead to higher efficiencies, though the difference is very slight. Nevertheless, the 10Ω gate resistor that was on the original boost converter will be replaced with a 1Ω gate resistor, and will remain so for the following tests.

Boost converters do not maintain a constant efficiency over their whole range of operation, thus there must be a certain load that will allow the boost converter to run most efficiently. The next series of tests will slightly increase and decrease the load resistor to see how

changing the load affects the performance of the boost converter in SPICE (Table 5.2). Some resistance values for the load resistor will make the converter pull enough current for the inductor core to saturate and cause its inductance value to drop, so the SPICE simulations have been modified with lower inductance values to more accurately simulate this phenomenon.

20Ω	91.93%	Input current is 2.74A, no modifications to inductor value
10Ω	95.43%	Input current is 5.22A, no modifications to inductor value
7Ω	95.72%	Input current is 7.36A, inductor value decreased to 3.9μH
7.5Ω	95.63%	Input current is 6.90A, inductor value decreased to 3.9μH
8.5Ω	95.47%	Input current is 6.12A, inductor value decreased to 4μH
8Ω (baseline w/ modified inductance)	95.58%	Input current is 6.49A, inductor value decreased to 4μH
5Ω	95.76%	Input current is 10.2A, inductor value decreased to 3.5μH

Table 5.2: Boost converter efficiency test with varying loads and compensated inductances

In reality, the saturation of the inductor is nonlinear and cannot be accurately simulated with a fixed inductor. However, looking at the change from the 20Ω to 10Ω to 8Ω load, it is clear that if the load is too small, the boost converter will not be hitting its max efficiency, and there seems to be a general trend of higher efficiency with a higher load. Thus, the strategy here is to load the boost converter just enough that the inductor barely hits saturation (defined when the inductance drops by 10%), resulting in the 7Ω resistor being chosen as the test load for the next simulation experiments.

Switching frequency is the final variable that can be controlled in order to observe its effects on efficiency. Tests were run while changing the switching frequency from the baseline 500kHz to 200kHz, 1 MHz, and 2MHz. Then a binary search was performed between the top

two performing frequencies to narrow down on a frequency that gives the highest efficiency (Table 5.3).

200kHz	91.23%
1MHz	95.85%
2 MHz	95.26%
1.25 MHz	95.74%
666.667 kHz	95.92%
800kHz	95.87%

Table 5.3: Testing efficiencies at different switching frequencies.

Based on all of the efficiency tests performed, it seems like the combination of a 1Ω gate drive resistor, 7Ω load resistor, and a switching frequency of 666.67kHz yields the best results at almost 96% simulation efficiency. The duty cycle is adjusted to bring the voltage within spec and the final expected specifications based on the simulation are detailed in Table 5.4.

Output Voltage (RMS)	23.88V
Output Voltage Ripple	40.17mV
Inductor Current Ripple	1.190A
Output Current (RMS)	3.412A
Input Current (RMS)	7.060A
Switching Frequency	666.67kHz
Duty Cycle	51%
Efficiency	96.17%

Table 5.4: Expected performance of finalized boost converter.

Performance of Physical Boost Converter:

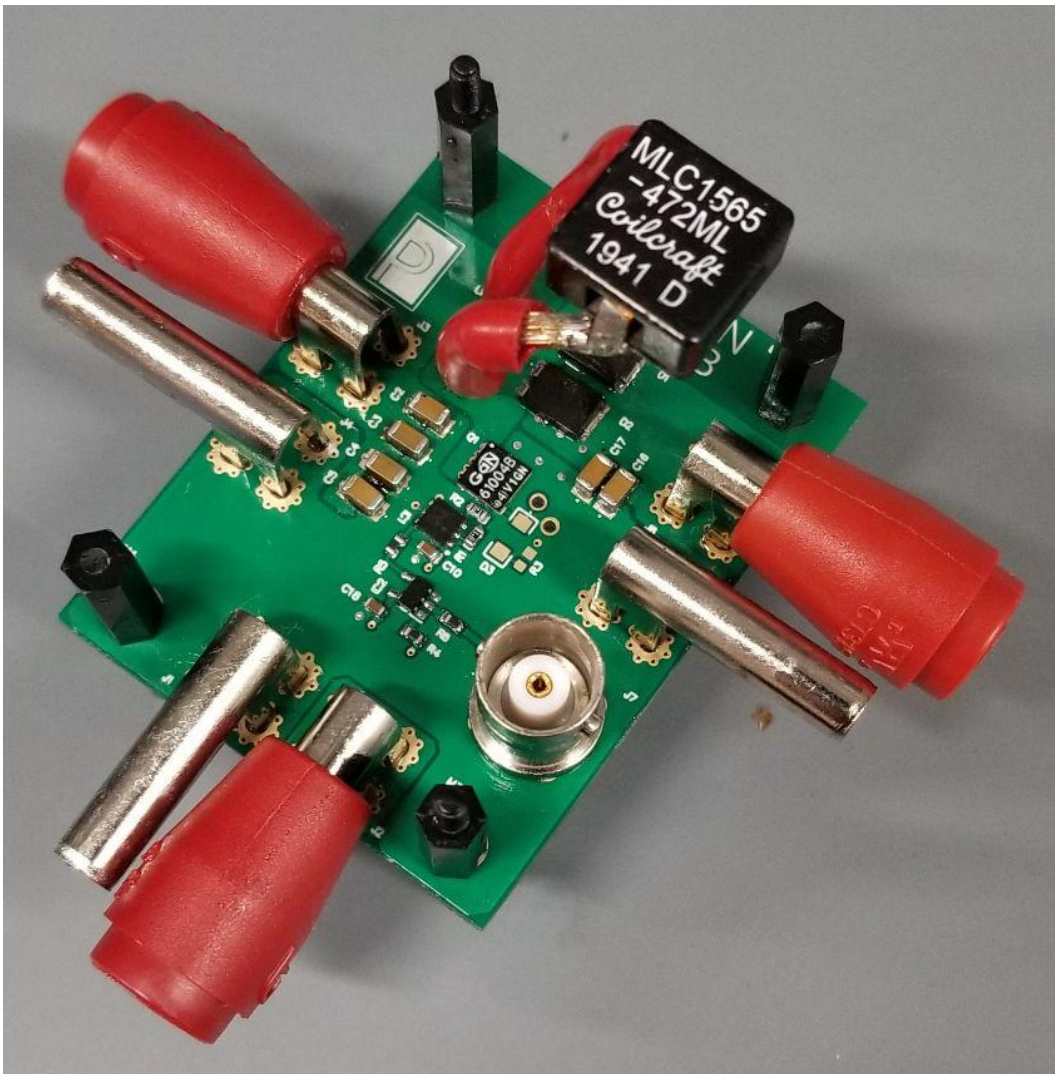

Figure 6.1: Completed boost converter

The real boost converter (Figure 6.1) was tested with an input voltage of 12V and an output load of 12Ω. Given this new data, the expected performance was recalculated using the formulas (Table 6.2) and the SPICE simulation was rerun (Table 6.3), obtaining new values. The values obtained from manual calculation and the simulation can be compared to the actual data gathered from the test (Table 6.3).

Output Voltage (RMS)	24.00V
Output Voltage Ripple (RMS)	23.12mV
Inductor Current Ripple	1.014A
Output Current (RMS)	2.000A
Input Current (RMS)	4.158A
Switching Frequency	666.67kHz
Duty Cycle	51.9%

Table 6.2: Performance values calculated from the formulas and model mentioned in section 2.

Output Voltage (RMS)	24.024V
Output Voltage Ripple	23.76mV
Inductor Current Ripple	1.020A
Output Current (RMS)	2.002A
Input Current (RMS)	4.2026A
Switching Frequency	666.67kHz
Duty Cycle	51%
Efficiency	95.37%

Table 6.3: Performance values obtained from the SPICE simulation

Output Voltage (RMS)	23.62V
Output Voltage Ripple	Practically None. (Very small)
Inductor Current Ripple	0.96A
Output Current (RMS)	1.97A
Input Current (RMS)	4.15A
Duty Cycle	51.8%
Efficiency	93.44%

Table 6.4: Actual performance values from the boost converter

Conclusion:

The actual performance of the boost converter regarding its input and output voltages and currents as well as the inductor ripple were very close to what was predicted in the mathematical models and simulations. The main factors that could have contributed to these differences include the parasitic inductances and resistances of the PCB, the heating of the inductor that could have affected the ESR, and the fact that a real inductor does not have a constant inductance for all currents. The efficiency of the real converter is less than the efficiency calculated in the simulation, but that is to be expected as the simulation only uses a linear model of the inductor and does not compensate for the changing ESR due to the transferred power.